KURZWEIL SC

DIGITAL SIGNAL PROCESSING COMPONENTS

KURZWEIL SEMICONDUCTOR KSC2408

PRELIMINARY

DIGITAL FILTER

Kurzweil Semiconductor

Features

- 8 programmable 2nd order digital filters
- 2 poles & 2 zeros per filter
- Internally cascadable to higher order filters
- 24 bit serial arithmetic & 48 bit accumulation
- 24 bit coefficients
- On chip rectification & decimation
- Fast mode of operation (higher sampling rate and reduced number of filters)
- Shared or independent data input
- Synchrony error detection
- Serial & parallel expansion
- On chip & across chip multiplexing
- Flexible configuration
- NMOS

Pin Configuration

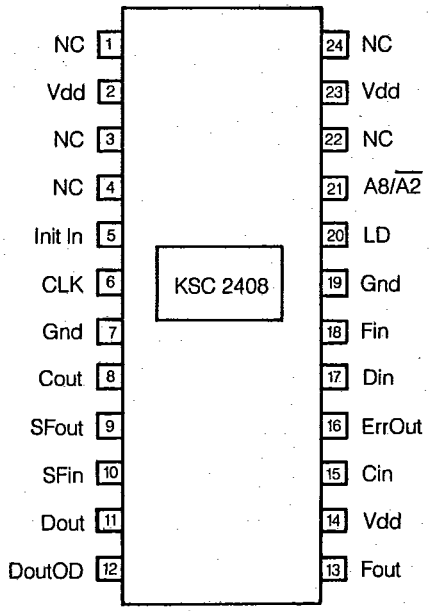
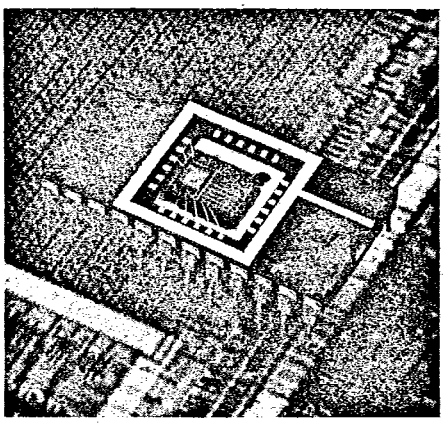


Figure 1

Part No.	Clock Rate (Typical)	Power Consumption (Typical)
KSC2408-6	6 MHz	.75 Watt
KSC2408-3	3 MHz	.60 Watt

Description

The KSC2408 is a general purpose programmable digital filter component consisting of 8 second order (2 poles, 2 zeros) filters which may be used independently, in parallel or cascaded. The architecture of the KSC2408 allows the designer to interconnect individual components to form arrays of filter banks. This device processes data using 24 bit coefficients with 24 bit I/O samples and 48 bits for internal accumulation. The device's bit serial architecture permits expanded capabilities to be integrated in a 24 pin package with only one input and one output data pin.



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Block Diagram

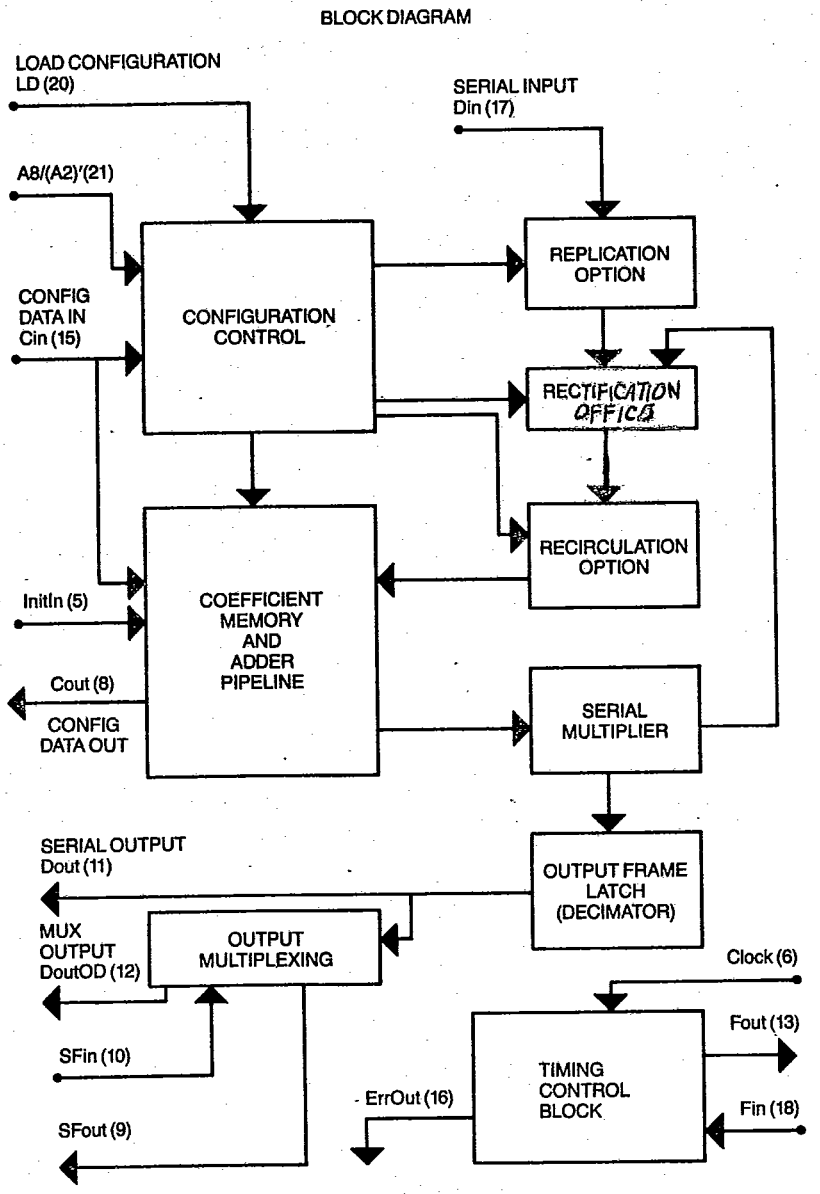


Figure 2

The KSC2408 comes in two versions, the KSC2408-3, which operates (typically) at 3 MHz, and the 6 MHz KSC2408-6.

The KSC2408 can be programmed to implement eight second order digital filters, which can be configured in many different ways, such as eight independent second order sections, four independent fourth order sections, two independent eighth order sections, or as one sixteenth order filter. Filtering with any one of these configurations takes place at a sampling rate of fs = (clock rate)/192. Thus, the 3 MHz version supports a sampling rate of 16 KHz.

Functional Description (continued)

Higher sampling rates can be attained by implementing only two out of the eight second order sections. These two sections can then be configured as two independent second order sections or as one fourth order filter. Filtering with any of these configurations takes place at a sampling rate of fs = (clock rate)/48, or four times faster than in the "eight filters" mode. These configurations are shown in Figures 3 and 4.

As can be seen from Figures 3 and 4, the KSC2408 features "on chip" multiplexing capabilities. The output of each second order section is internally multiplexed in a frame, as shown in Figure 5.

The KSC2408 can also do output decimation. The output can be decimated by any decimation factor from one to 256. This is useful when multiplexing several chips on one output line, as shown in Figure 6.

Two other features of the KSC2408 are input replication and input rectification. Although one chip can process as many as eight different independent channels, these channels can use the same input, if the input replication mode is selected. Input data can also be rectified before filtering, independently for each filter.

The KSC2408 can be cascaded to other KSC2408 chips to form higher order filters, as shown in Figure 7.

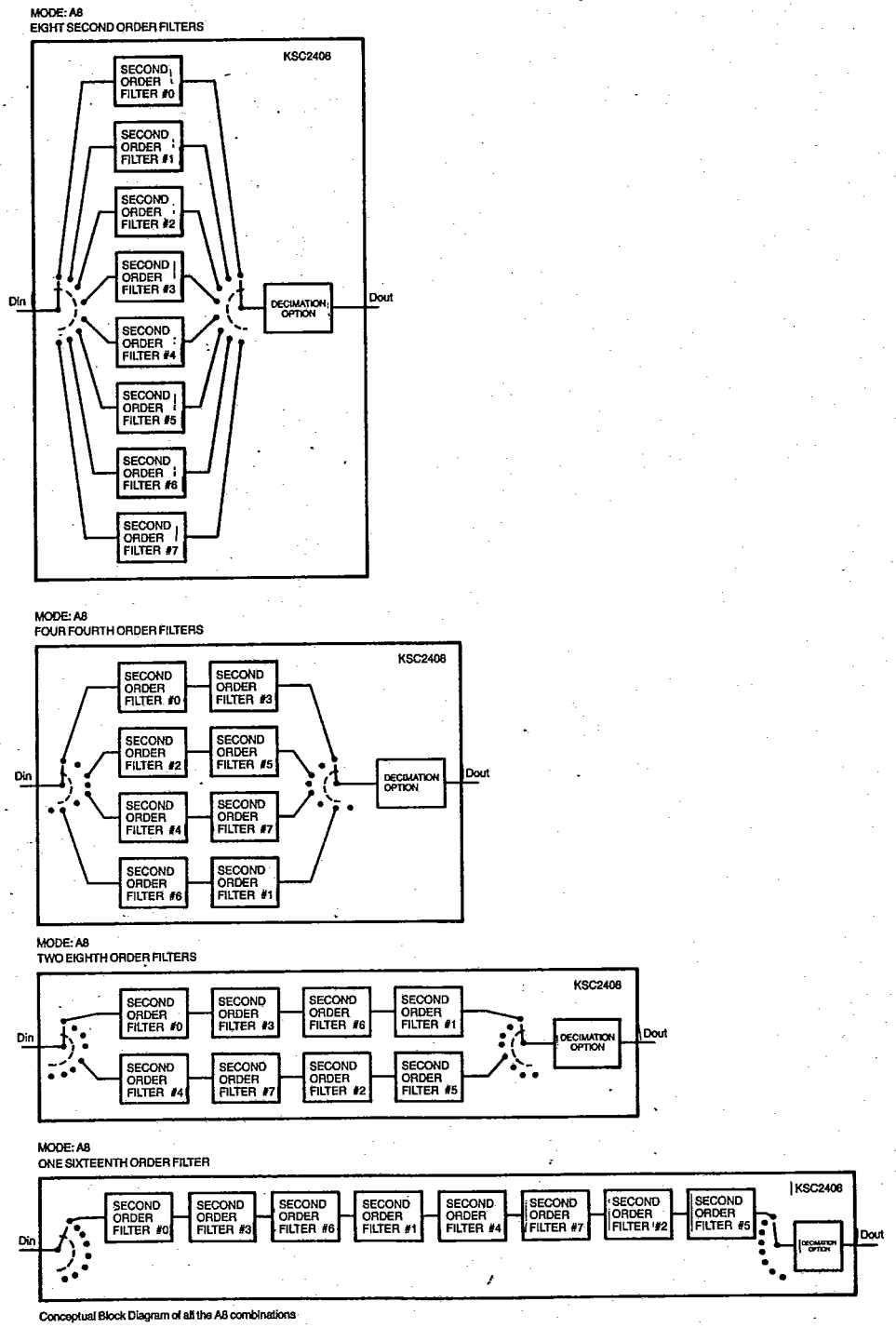
The KSC2408 is especially suited for use in multichannel filterbanks, as shown in Figure 8.

In order to lower the effective input sampling rate, the KSC2408 can freeze its internal state for a sample period. This is controlled by inputting a "null frame," that is, by suppressing the Fin (frame in) pulse at the start of a frame. (Shown in Figure 11.) Null frames do not have the Fout (frame out) pulse at the start of the output filtered frame, as valid data frames do.

The KSC2408 is configured or "programmed" by loading a bit serial configuration chain consisting of bits specifying the filter coefficients for all the filters being used (eight or two), and options such as master/slave control, output decimation, input rectification, internal cascading and input replication. 982 bits are used if eight filters are configured; 256 bits if only two filters are used. Figures 7 and 8 show two ways of configuring several KSC2408's.

The KSC2408 functions with standard TTL levels for I/O signals, power and ground.

A8 Configurations

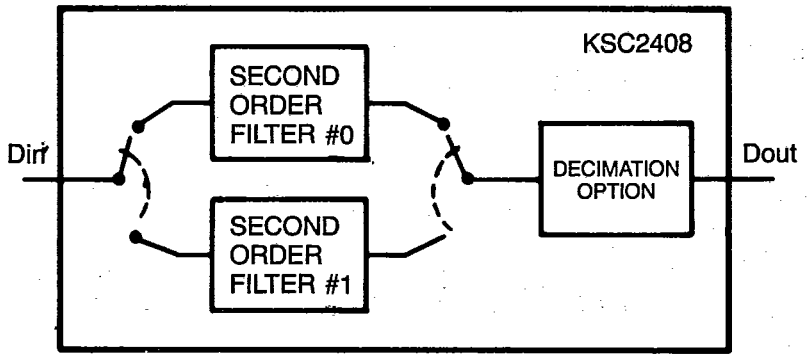


Conceptual Block Diagram of all the A8 combinations

Figure 3

A2 Configurations

MODE: A2
TWO SECOND ORDER FILTERS



MODE: A2
ONE FOURTH ORDER FILTER

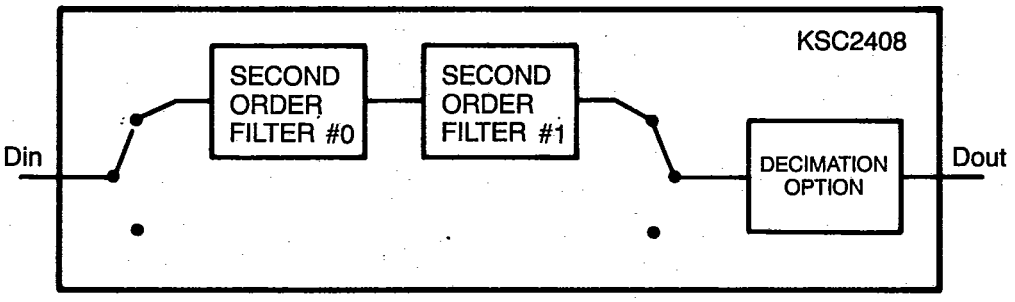


Figure 4

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PRELIMINARY

DIGITAL FILTERING

A digital filter is a system which modifies a given sampled data sequence (which can be a time series) referred to as the "input" into a desired sampled data sequence referred to as the "output". The input to output relationship is represented by the difference equation

$$Yn = \sum_{i=0}^{M} a_i x_{n-i} + \sum_{i=1}^{M} b_i Y_{n-i} \quad \text{..... (1)}$$

where Xn is the sampled data input and Yn is the output and M is the filter's order (having M poles and M zeros). By choosing the coefficients ai (i = 0,...,M) and bi (i = 1,...,M), as well as the order M in a judicious manner, we can control the frequency and time characteristics of the filter. The basic digital filtering system used in the implementation of high order filters is the second order section, also referred to as the biquadratic section (having 2 poles and 2 zeros). Implementation of higher order digital filters as a series of cascaded 2nd order sections reduces the effects of quantization noise (caused by the finite word length of the parameters, constants, and the internal arithmetic calculations) over that obtained in a direct form implementation.

The KSC2408 has two modes of operation, active eight (A8 and active two (A2)'. When used in A8 mode, the KSC2408 implements eight biquadratic digital filters which may be configured to operate in parallel or cascaded. When a KSC2408 is configured to be internally cascaded, it may form either one 16th order filter, or two parallel 8th order filters, or four parallel 4th order filters. When used in (A2)' mode (fast mode) only two of the eight biquadratic digital filtering sections are active, which results in a sampling rate four times that obtained when used in A8 mode. In (A2)' mode, the filters can be configured as two parallel 2nd order sections or one 4th order section; this is shown in Figures 3 and 4, respectively.

The KSC2408 can be used to form FIR filters (Finite Impulse Response) by making bi = 0 (i = 1,...,M). It can implement IIR filters (Infinite Impulse Response) by including the recursive terms in equation (1).

The sampling frequency at which the filters operate is given by

fs = sampling frequency = clock frequency / (24 * AF)

where AF is the number of active filters (eight or two).

The table of Filtering Configurations below gives the relationship between sampling frequencies and filtering configurations.

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DIGITAL FILTERING (continued)

FILTERING CONFIGURATIONS

PART	AF	fs max	I/O rate max	ORDER Configurations
KSC2408-3	2	64 KHz	3 MHz	one 4th, two 2nd
KSC2408-3	8	16 KHz	3 MHz	one 16th, two 8th, four 4th, eight 2nd
KSC2408-6	2	125 KHz	6 MHz	one 4th, two 2nd
KSC2408-6	8	31 KHz	6 MHz	one 16th, two 8th, four 4th, eight 2nd

The input to output difference equation of any one of the second order filters in the KSC 2408 is given by

$$Yn,f = \sum_{i=0}^{2} a_{i,f} x_{n-i} + \sum_{i=1}^{2} b_{i,f} Y_{n-i} \quad \text{..... (2)}$$

Where i is the coefficient index and f is the filter number (0, 1, ..., 7 for eight active filters, or f = 0,1 for two active filters). As shown by equation (2), there are five (24 bit) coefficients for each second order digital filter.

The filter coefficients take values in the range [−2, 2] covering all possible stable implementations (poles inside the unit circle). The coefficients are represented by 24 bits with a two bit integer part and a twenty-two bit fractional part. The internal arithmetic accumulation maintains 48 bits.

The input and output data consist of 24 bit numbers, represented in 2's complement notation. The input data should be scaled down to the range [−1, 1] so that the output data does not overflow 24 bits. Otherwise, this overflow will go undetected. An overflow will cause the data to "wrap around" which is typical to 2's complement arithmetic.

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PRELIMINARY

INPUT/OUTPUT DATA FORMAT

Data are represented in 2's complement notation as

$$X = -X^{\circ} + \sum_{K=1}^{23} X^{K} \cdot 2^{-K} \qquad (3)$$

where X^k represents the kth bit of data X. The data flow in and out of the KSC2408 is with the lsb (least significant bit) first followed by the next bit up to the msb (most significant bit) last.

The notation used for representing data in the KSC2408 is:

"Sample"	One 24 bit number.
"Frame"	Eight or two 24 bit numbers (depending on the A8/(A2)' setting). Input or output from all the filters on a single KSC2408.
"Superframe"	Output from several KSC2408s multiplexed onto one data line.

SAMPLE

| bit 23 | bit 22 | bit 21 | ..... | bit 0 |
lsb msb

FRAME (A8 mode)

| bit 23 | .... | bit 0 | bit 23 | .... | bit 0 | ..... | bit 23 | ..... | bit 0 |
[--- sample 0 ---] [--- sample 1 ---] ..... [--- sample 7 ---]

FRAME ((A2)' mode)

| bit 23 | ..... | bit 0 | bit 23 | ..... | bit 0 |
[--- sample 0 ---] [--- sample 1 ---]

SUPERFRAME

| frame 0 | frame 1 | ..... | frame N |

Data Format

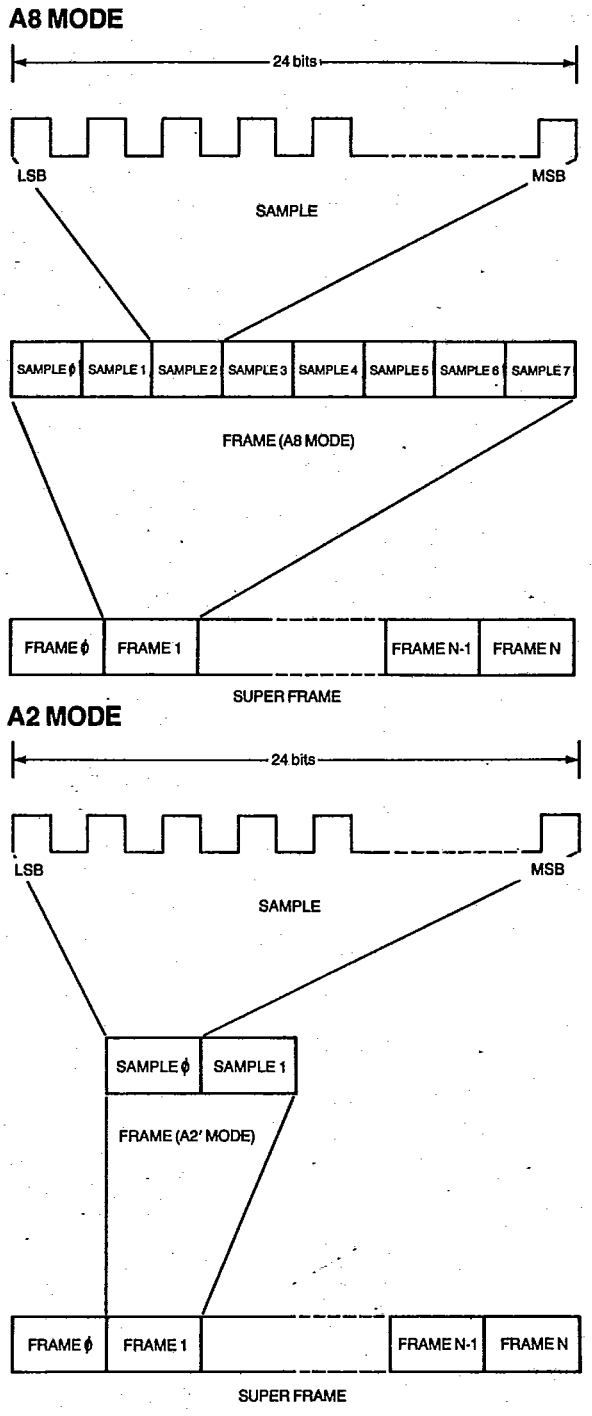

Figure 5

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PIN/FUNCTION DESCRIPTION

Pin No:	Name	Function
1, 3, 4, 22, 24	NC	These pins are not connected.
2, 14, 23	V_{DD}	Positive power pins (+5V) should have one common connection to the power line.
5	InitIn	InitIn pin should be grounded.
6	CLK	The input clock signal determines the rate at which data is processed.
7, 19	Gnd	Electrical ground (0 Volts) should be connected to one ground plane.
8	Cout	Cout (Configuration chain out). During a configuration load, the configuration bits "spill" out of Cout after a delay of 982 clock cycles for A8 or 256 for (A2), and can be fed to the Cin of another KSC2408.
9	SFout	Superframe output. This output is used when several KSC2408 outputs (decimated) are multiplexed into one line. SFout from one KSC2408 goes into SFin of the next one. A SFout pulse indicates to the next KSC2408 to be ready to dump its current frame into the multiplexed stream. The first KSC2408 in the series must have the "master" configuration bit set. All others are "slaves".
10	SFin	Superframe input. This input pin is used when several KSC2408 outputs (decimated) are multiplexed into one line, SFout from one KSC2408 goes into SFin of the next one. This pin must be grounded on the "master" KSC2408.
11	Dout	Data output line. Filtered data comes through this output pin formatted as a frame. A Fout pulse during the least significant bit of the first sample in a frame indicates that the frame from Dout is valid. A Fout pulse not present during the lsb of the first sample in a frame indicates that the present frame does not contain valid data.
12	DoutOD	Open drain, data output used as a "wired or" in multiplexing the outputs of several KSC2408s. DoutOD remains floating as long as the data out is invalid. When the data out is ready to be multiplexed then Dout and DoutOD have the same state (a 0 is low and a 1 is high).

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PIN/FUNCTION DESCRIPTION (continued)

Pin No:	Name	Function
13	Fout	Frame out. An output pulse is generated during the lsb of the first sample in a valid frame. This pulse serves as a synchrony indicator to pick the output data at the correct time. If Fout does not come at the beginning of a frame then the frame is a null frame and contains invalid data.
15	Cin	Cin (Configuration chain in) receives a configuration chain. The length of the configuration chain depends upon the mode of operation. The configuration chain is 982 bits when A8 is active, or 256 bits when (A2)' is active. The configuration consists of filter coefficients and I/O control bits (described below under Configuration Load). The configuration chain can be pipelined through several KSC2408s by connecting the Cout pin of one KSC2408 to the Cin of the next KSC2480 in the series (see Figure 8).
16	ErrOut	Error output. ErrOut indicates that an Fin frame pulse has been detected out of synchrony (anytime other than during the lsb of a frame. The output data might not be valid. Note: There is a mode of operation in which the user can tie Fin high and ignore the error line. In this mode the LSB of the first sample of data comes immediately on the first clock cycle when LD is low, and data comes continuously with no null frames.
17	Din	Data input line. This pin receives data for processing. Input data is presented in frame format with the least significant bit first. If the filters are configured to have common input, then all but the first sample in each frame will be ignored.
18	Fin	Frame pulse input. Whenever data is sent to the KSC2408 for processing, an input pulse must be present at Fin during the least significant bit of the first sample in the frame. If the pulse is not present during that time then a "null frame" or "freeze state" takes place, allowing a sampling rate reduction. This feature can be used to freeze the state variables when the next sample is not yet available. A Fin present anytime other than during the lsb of the first sample (one clock sample) triggers an error signal on ErrOut.
20	LD	Load configuration. This signal has to be active (set) during the loading of the configuration chain. The LD signal must be cleared before the first configuration bit corresponding to this KSC2408 is "spilled" out through Cout.
21	A8/(A2)'	A8 activates eight filters while (A2)' activates two filters (at four times the sampling rate of eight filters). The configuration length and the size of the frame depend on which mode (A8 or (A2)') is used.

CONFIGURATION LOAD

The KSC2408 filter coefficients and options are programmed by the configuration chain. The configuration chain can be pipelined through as many KSC2408s as desired in a single information stream line. The configuration load must occur before filtering. The configuration chain is programmed in the following sequence:

OUTPUT MULTIPLEX MASTER/SLAVE 1 BIT

When the output Multiplex configuration bit is set, the KSC2408 is configured as the controller or "master" of the multiplexing chain. If the bit is not set then the KSC2408 is configured as a slave. When configured to decimate, the KSC2408 has an internal clock which controls the latching of the appropriate frame. The decimation factors of all KSC2408s in the chain must be the same. On the "master" KSC2408 the SFin pin must be grounded. The "master" generates a SFout high signal during the least significant bit of its current frame which lasts until the lsb of the next frame. The SFout signal is sent to the SFin pin of the next KSC2408 and serves as an "output enable" control signal. The receiving KSC2408 transmits its latched frame during the lsb of the next frame and raises its SFout during its least significant bit. This SFout signal goes to the next KSC2408 and the process is replicated for all multiplexed KSC2408s. Any "slave" KSC2408 dumps its latched superframe to the next frame after receiving a SFout signal from the KSC2408 that drives it, Figure 6 depicts three KSC2408 multiplexed, the top-most KSC2408 is configured as a "master" while the rest are configured as "slaves," the multiplexed line is Dout OD.

NOTE: A chain of multiplexed KSC2408's can be as long as the decimation factor.

The KSC2408 has an output pin (Dout), and a "wired or" output pin (DoutOD) which serves as an open drain line with an external pull-up resistor. The DoutOD line stays high (floating) during its inactive state and replicates the Dout line when it is ready to transmit data. The DoutOD outputs of several KSC2408's are tied together and effectively "wire or" the data outputs for multiplexing (see Figure 6).

DECIMATION FACTOR 8 BITS

Decimation involves keeping every Nth sample (where N is the decimation factor) and discarding all other samples. The output decimation factor consists of 8 bits with the msb first and lsb last. The decimation factor assumes values between 1 (no decimation) and 256.

CONFIGURATION LOAD (continued)

FILTER COEFFICIENTS
960 BITS on Active 8, 240 BITS on Active 2

Filter coefficients are specified in the configuration chain in the following order [see equation (2) above]. The number of active filters is AF (2 or 8).

[lsb(b1,0)], [lsb(b1,1)],.....[lsb(b1,AF-1)] .....
..... [msb(b1,0)], [msb(b1,1)],.....[msb(b1,AF-1)],
[lsb(b2,0)], [lsb(b2,1)],.....[lsb(b2,AF-1)] .....
..... [msb(b2,0)], [msb(b2,1)],.....[msb(b2,AF-1)],
[lsb(a2,0)], [lsb(a2,1)],.....[lsb(a2,AF-1)] .....
..... [msb(a2,0)], [msb(a2,1)],.....[msb(a2,AF-1)],
[lsb(a1,0)], [lsb(a1,1)],.....[lsb(a1,AF-1)] .....
..... [msb(a1,0)], [msb(a1,1)],.....[msb(a1,AF-1)],
[lsb(a0,0)], [lsb(a0,1)],.....[lsb(a0,AF-1)] .....
..... [msb(a0,0)], [msb(a0,1)],.....[msb(a0,AF-1)],

A coefficient bi,L represents the coefficient of Y_{n-i} for filter L and a coefficient ai,L represents the coefficient of X_{n-i} for filter L.

RECTIFICATION ENABLE
8 BITS on Active 8, 2 BITS on Active 2

Full wave rectification (obtain the absolute value) of the input to any filter is accomplished by setting the corresponding bit high. The format is

[bit 0],.....,[bit AF-1]

If a bit is cleared, the corresponding filter input is not rectified.

RECIRCULATION PASSES 4 BITS

These 4 bits are presented with the msb first. Only one of the four bits can be high, indicating 1, 2, 4 or 8 recirculation passes, where the number of recirculation passes corresponds to the number of second order stages being cascaded to form higher order filters. The input and output data to the KSC2408 are every Nth sample in the frame (N = number of recirculation passes), unless the common input mode is selected, in which case the first sample in the frame is used as the input to all of the filter chains. The input to output pipeline delay (from Fin to Fout) depends on the recirculation factor. The delay is given by:

pipeline delay = 9 + 72*N clock cycles

where N = 1, 2, 4, or 8 recirculation passes.

CONFIGURATION LOAD (continued)

1 pass → eight or two, second order filters (A8 or (A2)')

2 passes → four or two, fourth order filters (A8 or (A2)')

When Active 8, the data in and out from the four filters is in samples 0, 2, 4, 6 in the frame.

When Active 2, the data in and out from the two filters is in samples 0 and 2 in the frame.

4 passes → 2 eight order filters (A8)

The data in and out from the two filters are samples 0 and 4 in the frame.

8 passes → 1 sixteenth order filter (A8)

The data out comes from sample 0 of the output frame and the data in is contained in sample 0 of the input frame.

To configure the filter coefficients into the configuration chain when recirculation (internal cascading) is used, KSC-supplied software assigns the filter coefficients in the configuration chain as outlined below.

Two recirculation passes are used to form four 4th order filters in the following manner:

1st Section	2nd Section
filter 0	filter 3
filter 2	filter 5
filter 4	filter 7
filter 6	filter 1

Four recirculation passes are used to form two 8th order filters in the following manner:

1st Section	2nd Section	3rd Section	4th Section
filter 0	filter 3	filter 6	filter 1
filter 4	filter 7	filter 2	filter 5

Eight recirculation passes are used to form one 16th order filter in the following manner:

CONFIGURATION LOAD (continued)

1st Section	2nd Section	3rd Section	4th Section	5th Section	6th Section	7th Section	8th Section
filter 0	filter 3	filter 6	filter 1	filter 4	filter 7	filter 2	filter 5

As mentioned above, input and output data are available every Nth sample in a frame, where N is the number of recirculation passes.

REPLICATED INPUT 1 BIT

When the replicated input bit is set, sample 0 in the input frame is replicated to all filters on the KSC2408, disregarding other samples in the input frame. When the replicated input bit is cleared, each filter receives the corresponding sample from a frame.

The total number of configuration bits is:

	Active 8	Active 2
Output MUX	1	1
Decimation Factor	8	8
Coefficients	960	240
Rectification	8	2
Recirculation	4	4
Replicated Input	1	1
TOTAL	982 BITS	256 BITS

APPLICATIONS

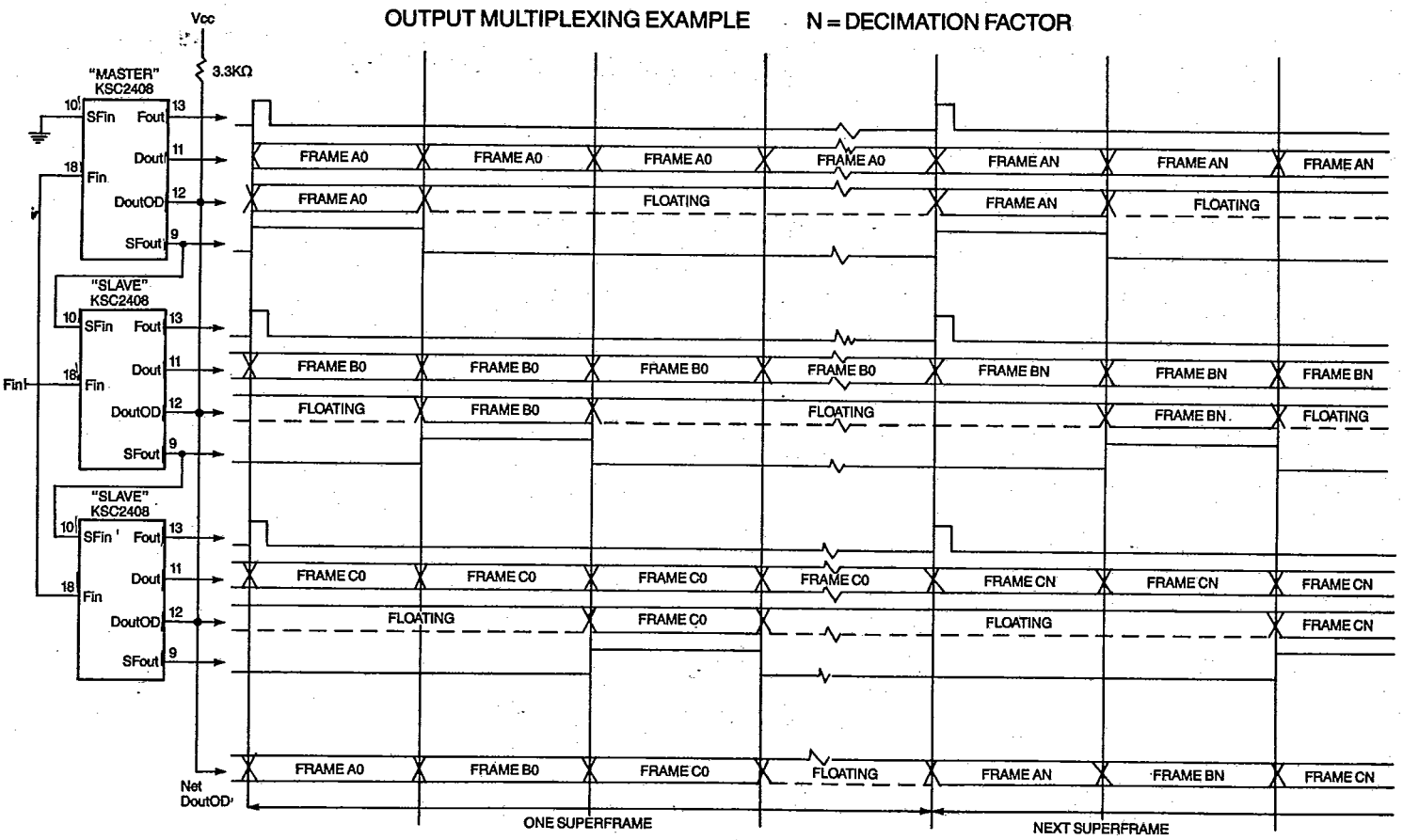

Figure 6

CASCADED CONFIGURATION
NIBBLE LOAD

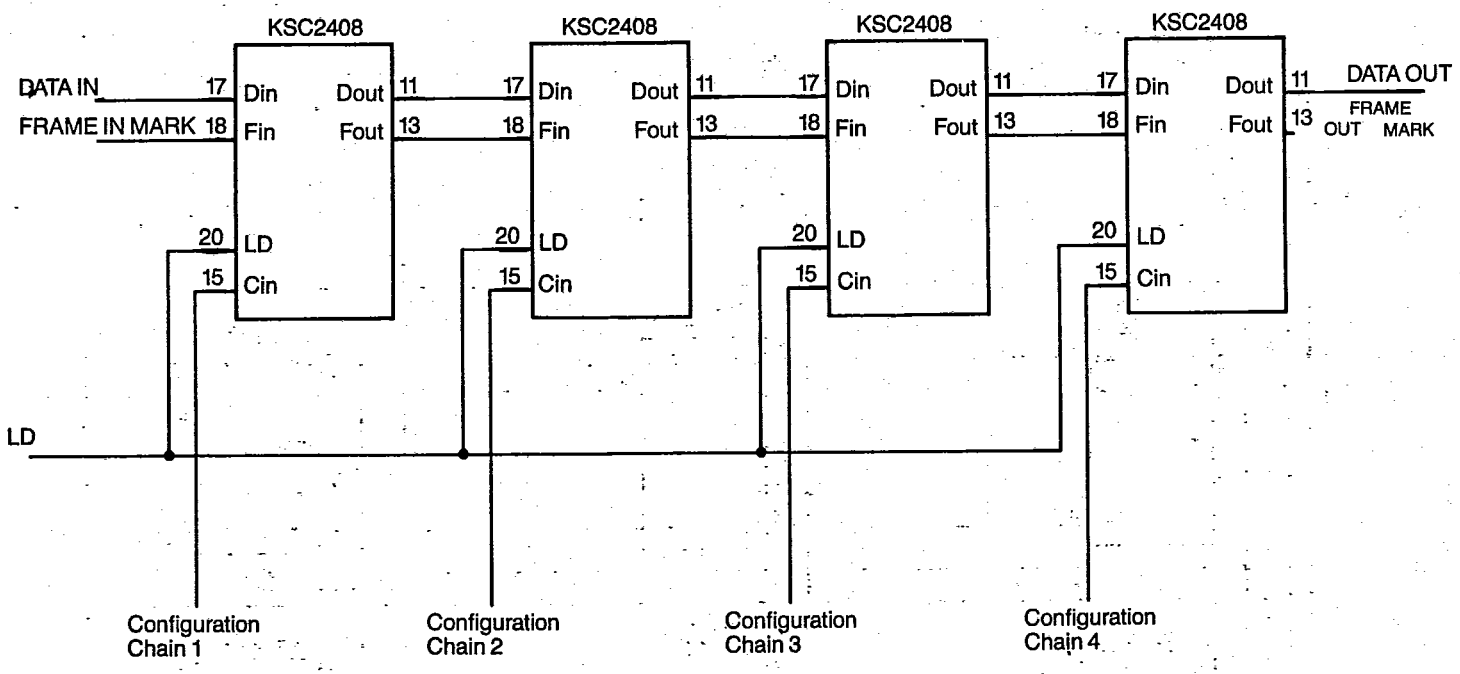

Figure 7

KURZWEIL SC

DIGITAL SIGNAL PROCESSING COMPONENTS

KURZWEIL SEMICONDUCTOR KSC2408

PRELIMINARY

DIGITAL FILTER

FILTERBANK ARRAY

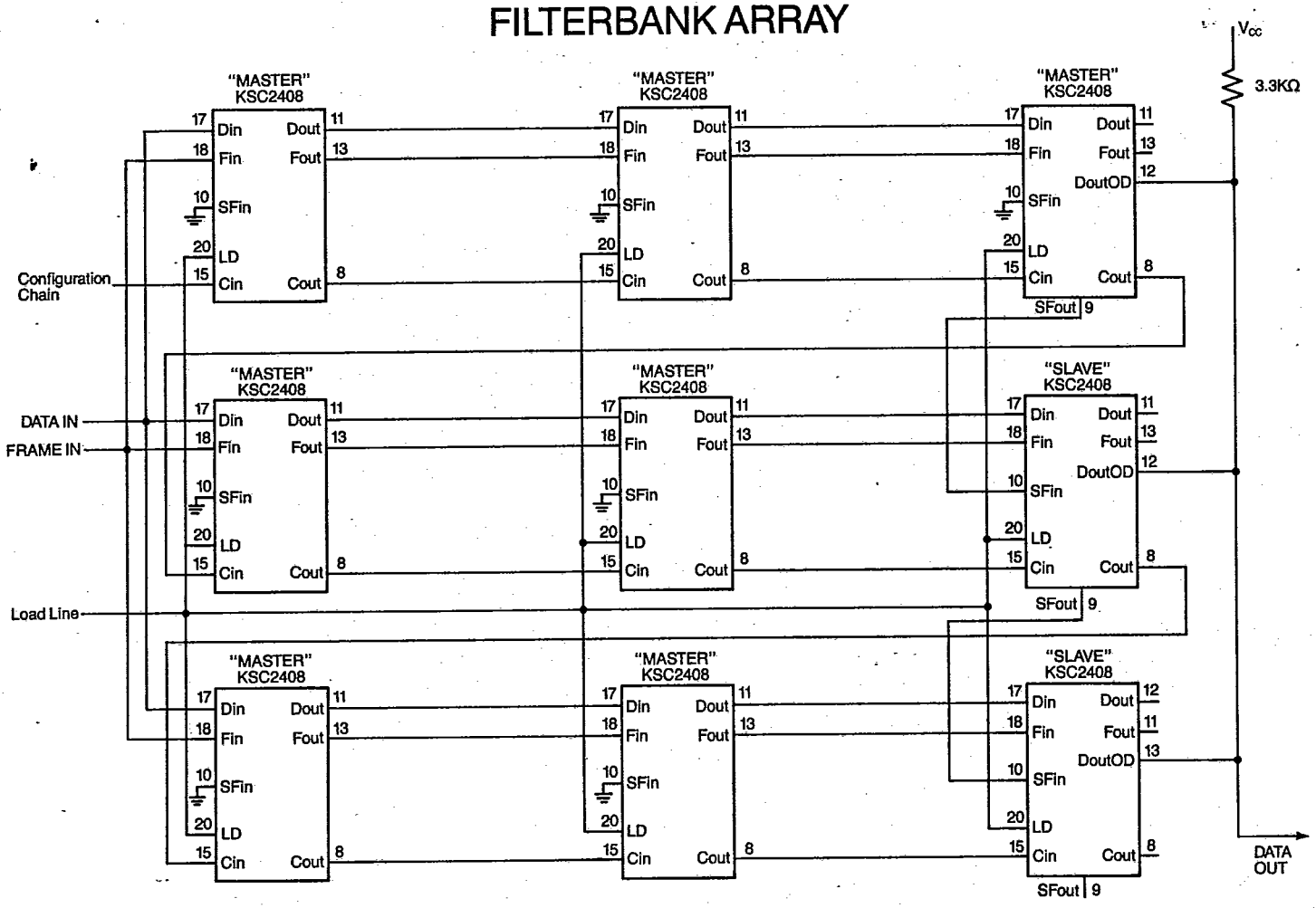

Figure 8

LOADING CONFIGURATION

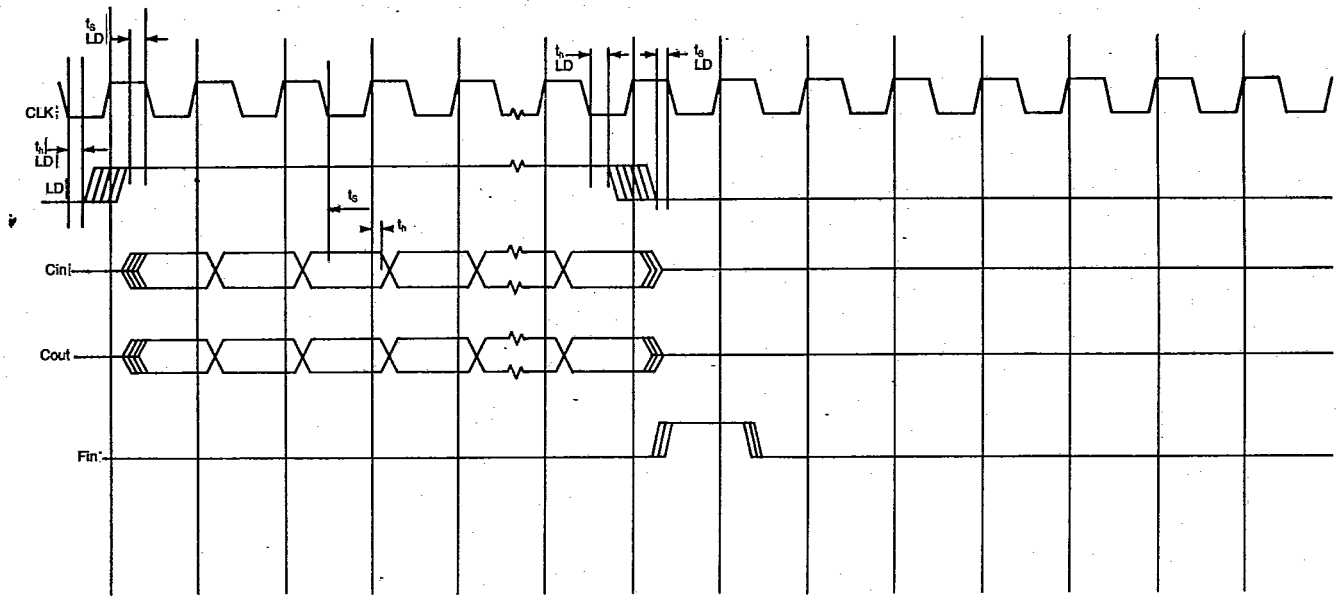

Figure 9

FILTERING

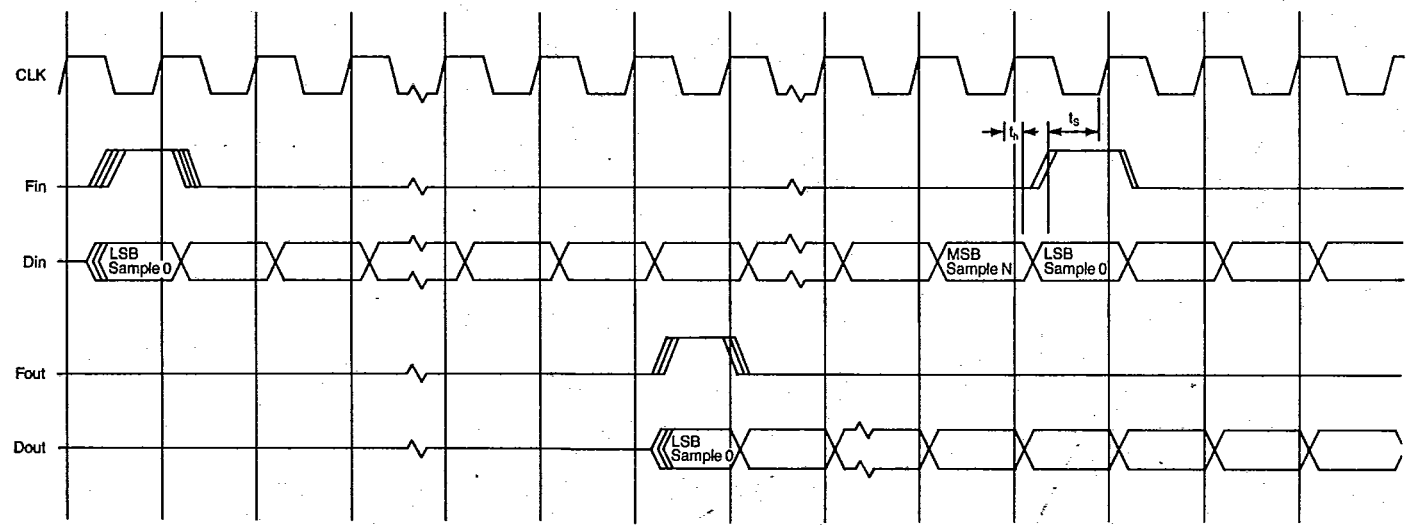

Figure 10

Null Frames (A8 Mode)

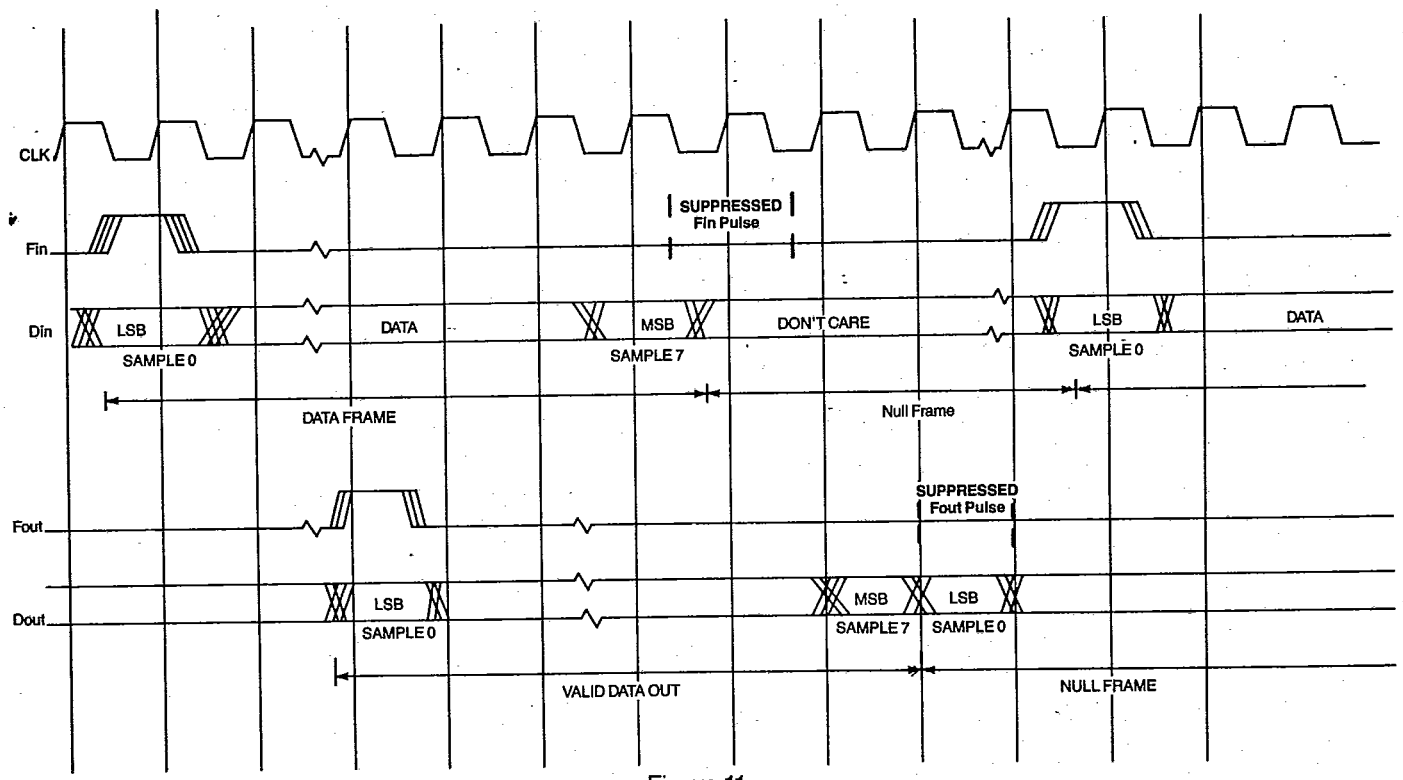

Figure 11

ERROR DETECTION

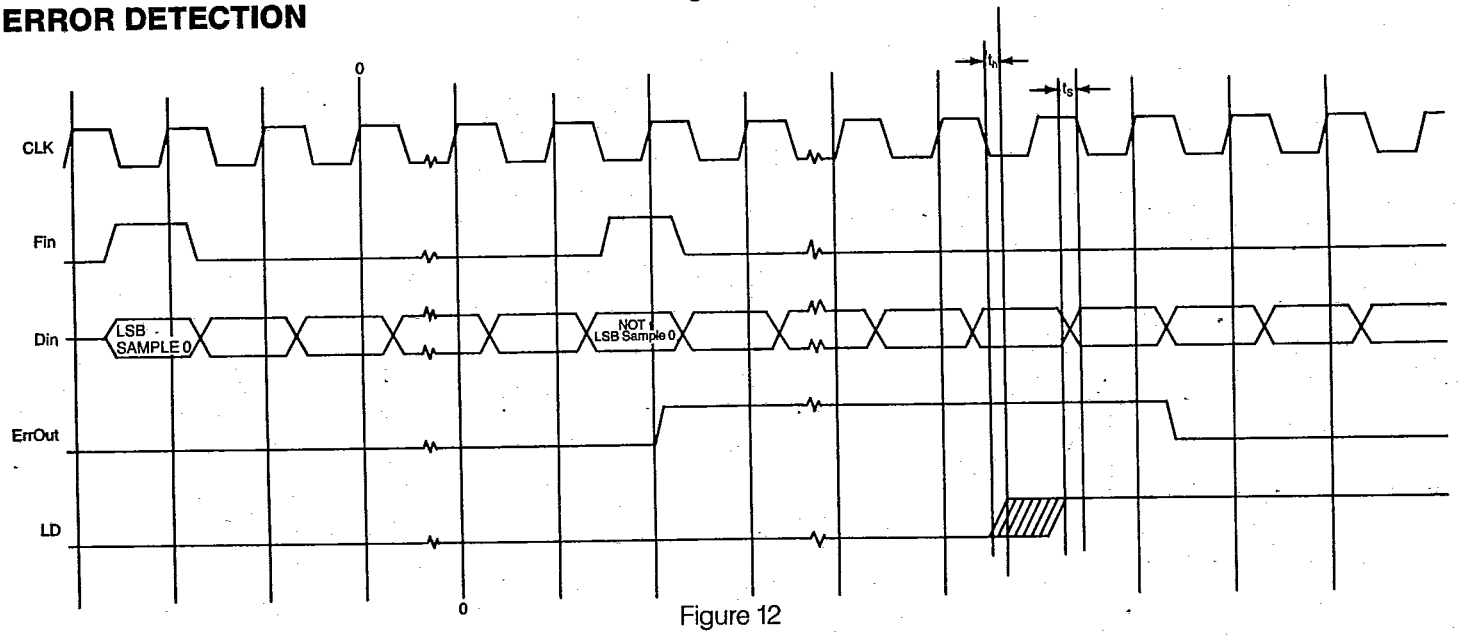

Figure 12

I/O TIMING DETAIL

This diagram describes in detail, I/O DATA TRANSITIONS

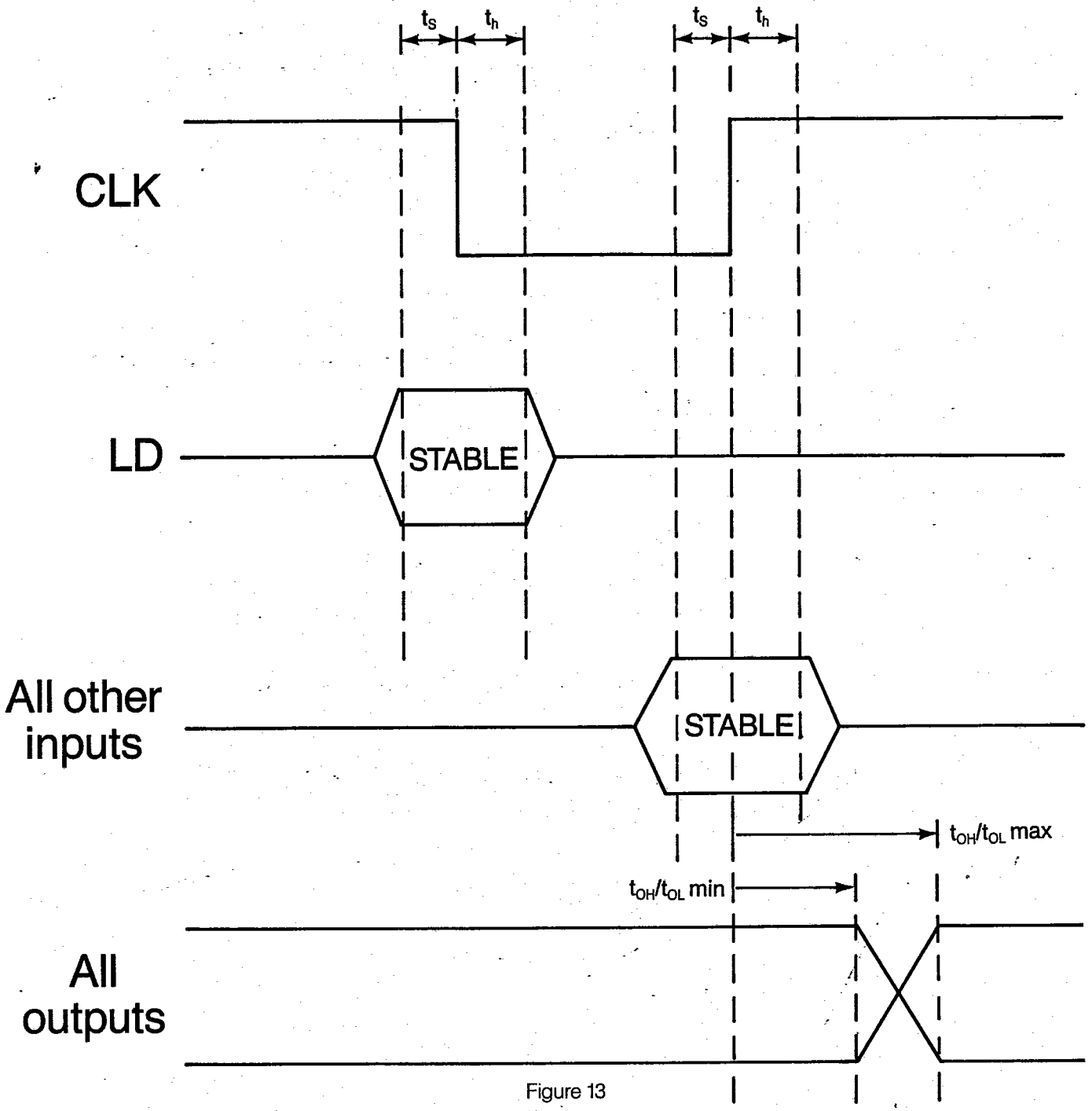

Figure 13

KURZWEIL SC

PRELIMINARY

OPERATING CHARACTERISTICS

Parameter	KSC 2408-3 min	KSC 2408-3 max	KSC 2408-3 typical	KSC 2408-6 min	KSC 2408-6 max	KSC 2408-6 typical
TA	0°C	70°C	25°C	0°C	70°C	25°C
CLK (MHz)	.024	3.0	—	.024	6.0	—
Vdd	4.5	5.5	5.0	4.5	5.5	5.0
Power (Watt)			.60			0.75

All I/O signals are standard TTL.

$i_{source} = 1.6$ mAmp

	KSC2408-3	KSC2408-6
$t_{settling_{min}}$	40 nsec	40 nsec
$t_{settling_{max}}$	80 nsec	100 nsec
Temp	27°C	70°C
$T_{LF_{max}}$	.25 sec	8 m.sec

T_{LF} — time interval between the end of the load and the start of the first frame (Fin).

Note: If T_{LF} is violated the configuration may be lost.

A.C. Characteristics (VDD = 5V, TA = 25°C)

Capacitance 50 pf load on each output chip

KURZWEIL SC

SWITCHING CHARACTERISTICS

(time in 1×10^{-9} sec, KSC2408-3, KSC2408-6)

Signal	$t_{h\,max}$	ts	t_{OH}/t_{OL} min	max
SFin	30	20	—	
Cin	30	20	—	
Din	30	20	—	
Fin	30	20	—	
LD	30	20	—	
A8/A2'	30	20	—	
SFout	—	—	40	80
Cout	—	—	40	80
Dout	—	—	40	80
DoutOD	—	—	40	80
Fout	—	—	40	80
ErrOut	—	—	40	80

NOTE: Output Signals (sush F_{out}) should not be used as a clock (strobe).

NOTES

1. KSC will provide configuration sample programs to load a series of filters with the desired coefficients and configuration.

2. A stand-alone filtering evaluation and development board with one KSC 2408 and parallel I/O (24 bits) is also available.